REMARKS

No claims have been added, cancelled, or amended. Claims 25-30 are pending.

Claims 25-27 and 30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner (U.S. Patent No. 5,899,721) in view of Mogami (U.S. Patent No. 5,656,519). Claims 28-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner, Mogami, and Bai (U.S. Patent No. 5,861,340). These rejections are respectfully traversed.

Referring to Figs. 4-9 the semiconductor device of the present invention includes a gate electrode stack 10 disposed upon a dielectric film 16 over a portion of a wafer, such as substrate 17. The gate stack 10 includes a plurality of layers, for example, layers 11, 12, 13, 14, and 15. Above the gate stack 10 is an oxide cap 20. In one embodiment, the electrode stack 10 includes a polysilicon layer 11 and at least one metal layer 13. As shown in the figures, the sidewalls 18 of the electrode stack are continuously vertical. Surrounding the sidewalls 18, continuously from the bottom to the top of the sidewalls 18 are composite spacers, each of which comprise a nitride spacer 22 stacked above an oxide spacer 20. The oxide spacer 20 extends from at least a bottom most portion of the continuously vertical sidewalls 18 to an intermediate point between the bottom most portion of the sidewalls 18 and a top point of the sidewalls 18. The nitride spacer 22, which is formed after the oxide spacer 20 is formed, extends from the intermediate point to the top of the sidewalls 18.

Accordingly, claim 25 recites:

> a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls,
>
> wherein each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer,
>
> said oxide spacer extending along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls, and said nitride space spacer extending from the intermediate point to the top of said continuously vertical sidewalls.

Gardner is directed at a method of forming small spacers, as illustrated by Fig. 9. Gardner teaches a semiconductor device including a stack, which is comprised of a gate oxide (Fig. 9, layer located immediately under 104), a polysilicon gate conductor 104, and a metal silicide 122. Gardner discloses the forming a composite spacer along a continuously vertical sidewall with the composite spacer having a nitride layer 114 over an oxide layer 116. As shown in Fig. 9, the composite spacer fails to "extend continuously from a bottom to a top of said continuously vertical sidewalls," as required by claim 25.

Mogami is directed to a method of manufacturing a MOS device having a gate electrode and source/drain regions. Referring to Fig. 8a, Mogami discloses the formation of a gate electrode stack by depositing: a gate oxide layer 5, a polysilicon layer 6', a tungsten nitride layer 31, and a second polysilicon layer 32. In Fig. 8B, a simple (i.e., single material, or non-composite) oxide spacer 9 is formed which spans the sidewalls of the electrode stack under construction (i.e., layers 5, 6', 31, and 32). In Fig. 8C, the polysilicon layer 32 of the electrode stack under construction (only) is removed, thereby

causing the top portion of the oxide spacer 9 to exceed the height of the top portion of the electrode stack under construction (which now has a top at layer 31). In Figs. 8D, 8E, and 8F, a titanium layer is deposited and reacted, the unreacted portions of the titanium layer are removed, and finally a tungsten layer is deposited, respectively. The completed device is illustrated in Fig. 8F, and still retains an oxide sidewall 9 higher than the top of the electrode stack (now tungsten layer 33). Mogami further discloses that having an oxide spacer which extends above the height of the gate electrode stack electrically isolates the gate electrode stack from the source/drain regions and therefore is advantageous in preventing short circuits between the gate electrode stack and the source/drain regions. Column 8, lines 5-15.

Mogami fails to disclose or suggest "a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls, wherein each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer," as required by claim 25. Mogami further fails to disclose or suggest "said oxide spacer extending along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls," which is also required by claim 25.

Bai is cited by the Office Action for its teaching of a refractory silicide metal layer, a diffusion layer, and a barrier layer which is substantially impermeable to silicon and metal atoms. However, Bai does not teach or suggest a gate electrode stack and an associated composite spacer having the above described limitations of claim 25.

The Office Action alleges that it would be obvious to "form the spacer structure extending from a bottom to over a top of the continuously vertical sidewalls of [the] gate electrode stack as taught by Mogami into Gardner et al.'s device in order to prevent the short circuit between the source/drain regions and gate electrode stack." However, such a conclusion is defective for at least the following reason. The spacer structure of Gardner is a composite oxide-nitride spacer while the spacer of Mogami is a simple oxide spacer. If the oxide portion of the composite spacer were lengthened as suggested to achieve the benefit taught by Mogami there would be no need for the nitride portion of the spacer. Further, even if the teachings of Mogami were adopted into the device of Mogami, the resulting structure would include a sidewall having an oxide layer which ran from at least a bottom to above a top of said structure. Such a structure, contrary to the assertion made in the Office Action, would not be the claimed structure because the claim 25 requires the oxide spacer to "extend[ing] along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls."

The Office Action further argues that Mogami's teaching should be extended to include that using any type of sidewall which has a height exceeding that of the electrode stack would be advantageous by electrically isolating the gate electrode stack from the source/drain regions, and thereby reduce the possibility of shorting between a source/drain region and the gate electrode stack. Although applicant's representative believes this is an inappropriate conclusion to draw from Mogami, it should be noted that even if this teaching is adopted, there would be no reason to incorporate the teaching into

the device of Gardner as suggested by the Office Action. This is because Gardner already includes a mechanism for avoiding short circuits between source/drain regions and the gate electrode stack. As shown in Fig. 9, the source/drain regions 120 and the top of the gate electrode stack are enclosed by metal silicide layers 122. The metal silicide layers 122 are formed in a process described at column 7, lines 12-41. More specifically, Gardner states at column 7, lines 33-41:

The resulting metal silicide 122 has a relatively low resistivity and serves as a self-aligned contact region across source/drain regions 120 and gate conductor 104. Absent refractory metal upon the lower portions of the spacers, no silicide formation occurs at those potions. Consequently, silicide bridging between gate conductor 104 and source/drain regions 120 is less likely to occur. Since Gardner already incorporates this mechanism to prevent short circuits between the gate electrode stack and source/drain regions, there would be no reason to incorporate the mechanism from Mogami for performing the same function.

Claim 25 is therefore believed to be allowable over the prior art of record. Claims 26-30 depend from claim 25 and are believed to be allowable over the prior art of record for these reasons and because the combination defined in the claims is not shown or suggested by the cited references.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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